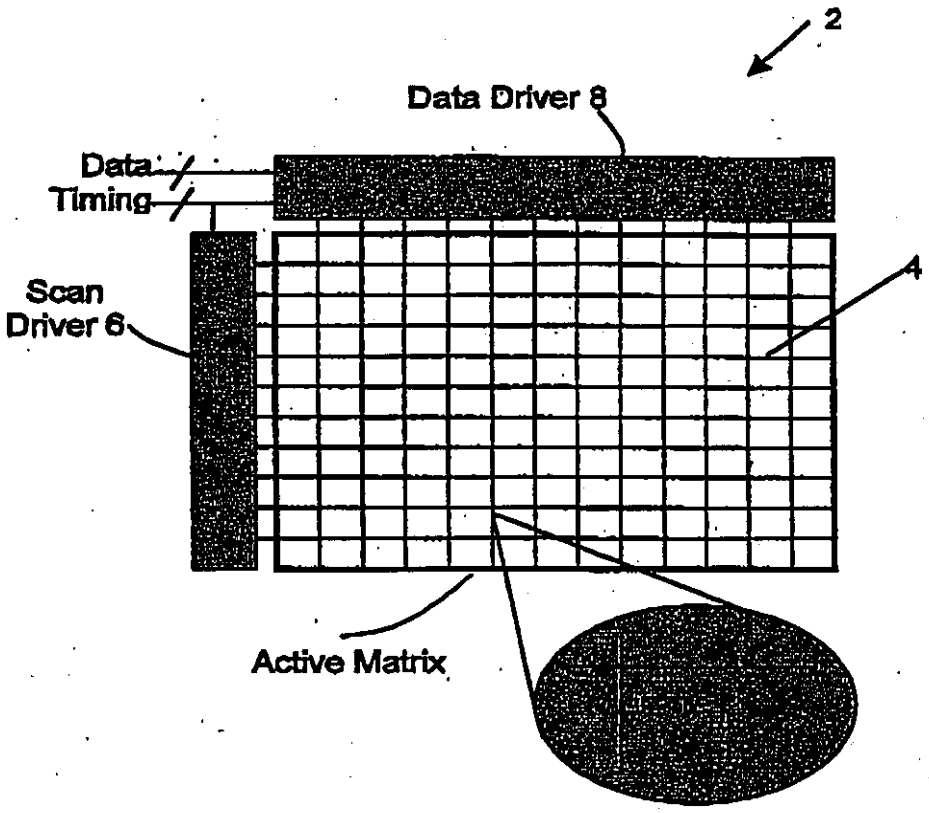


**Figure 1: Prior art - Typical Active Matrix Display**

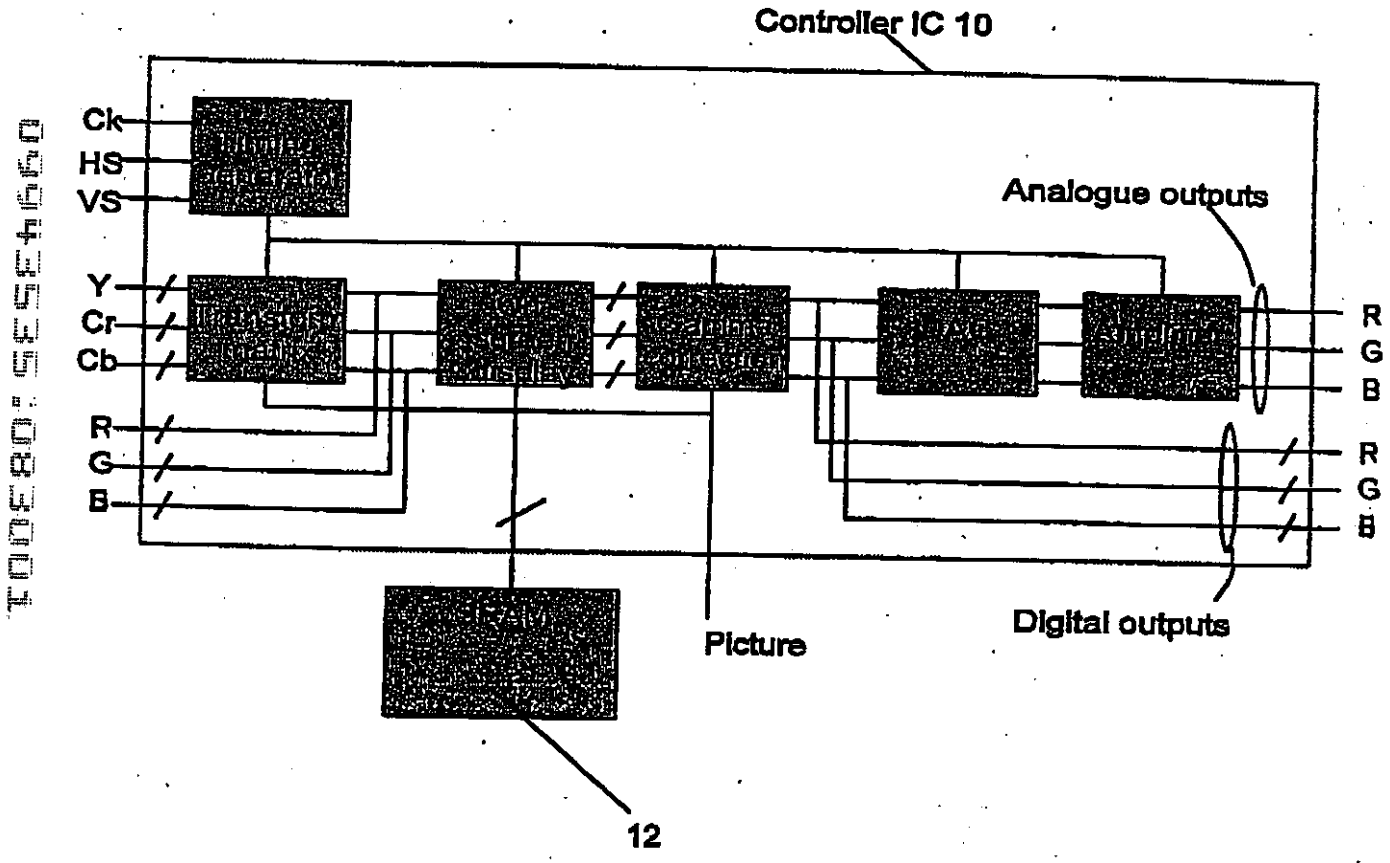


Figure 2 prior art - typical active matrix display controller IC

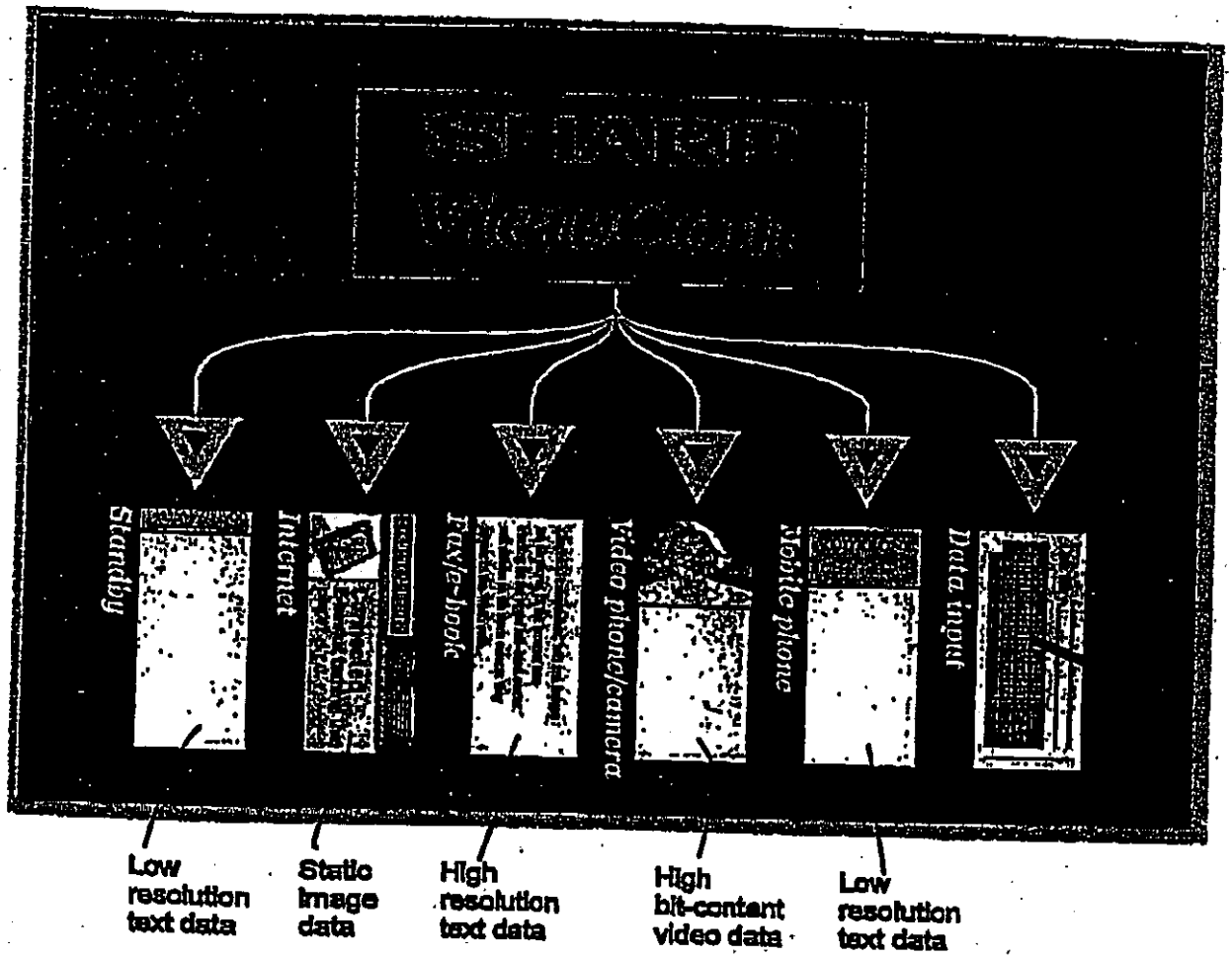


Figure 3: Conceptual application of multi-format image data

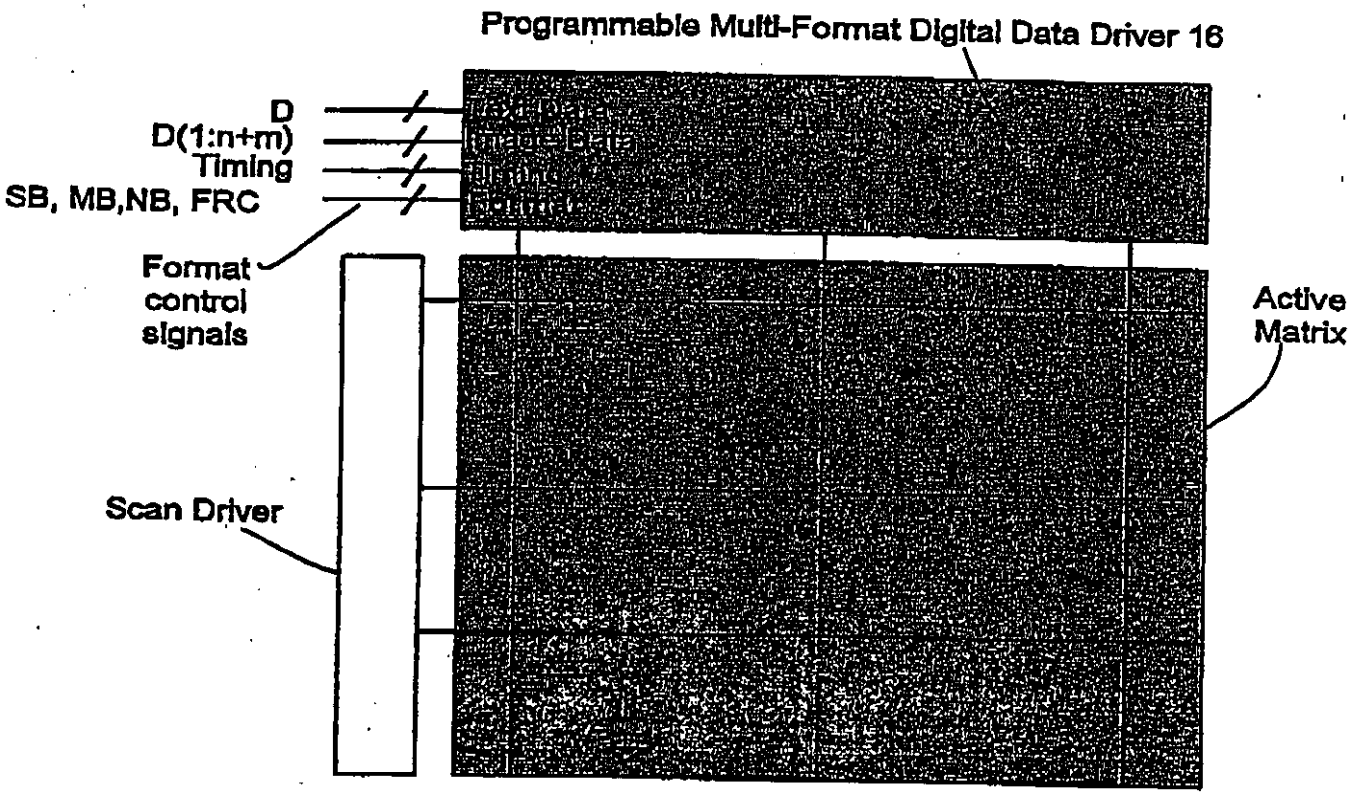


Figure 4: Multi-format digital data driver

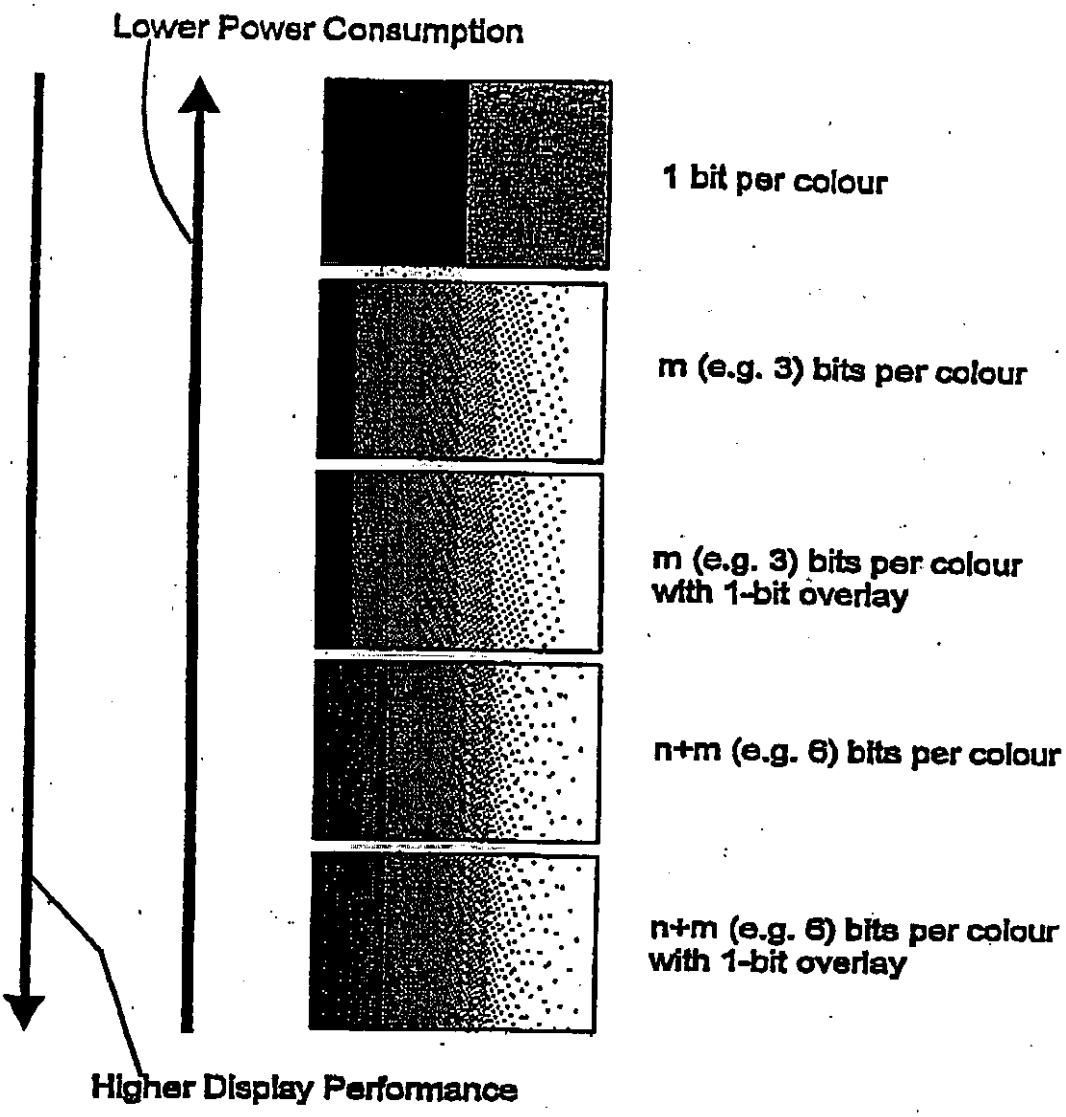


Figure 5: The trade-off between power consumption and image quality

| Format Control | | | |
|---|---|---|---|
| NB | MB | SB | Driver Format |
| 0 | 0 | 1 | 1-bit per colour |
| 0 | 1 | 0 | m bits per colour |
| 1 | 1 | 0 | n+m bits per colour |
| 0 | 1 | 1 | m bits per colour with 1-bit overlay |
| 1 | 1 | 1 | n+m bits per colour with 1-bit overlay |

Figure 6: Table showing three Format Control Signals and selected format

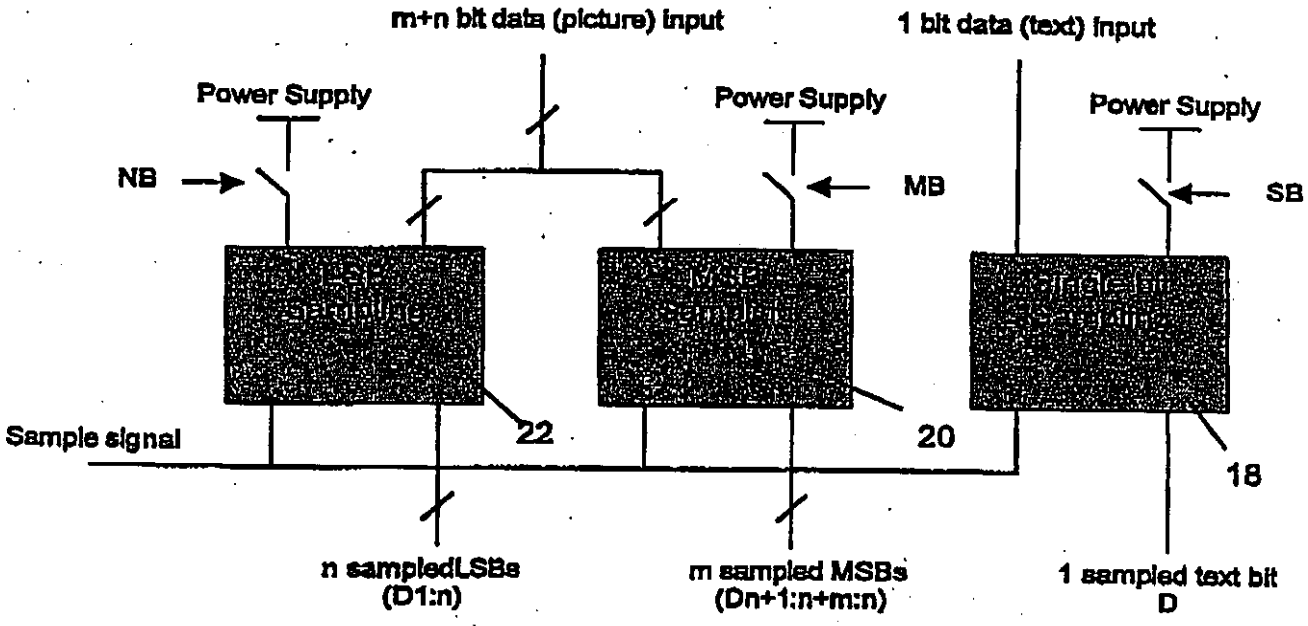


Figure 7: Power control within data sampling unit of multi-format driver

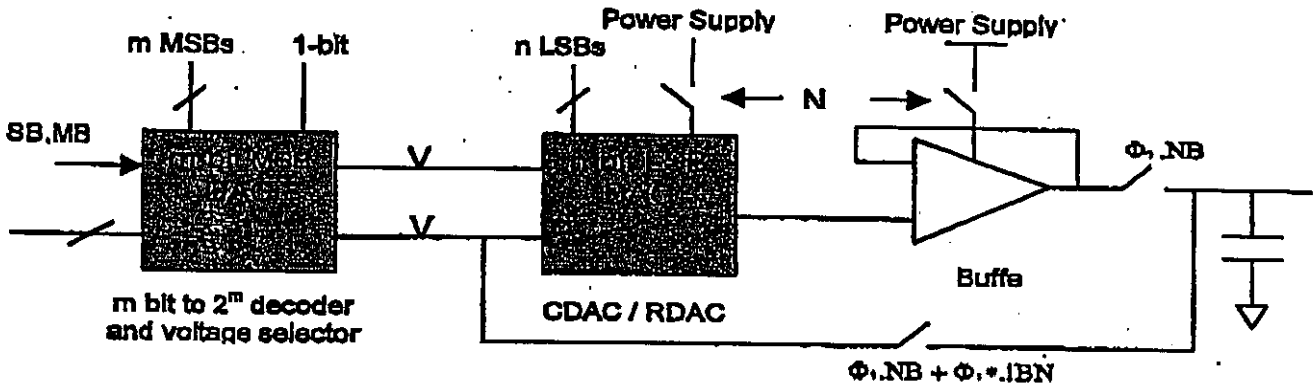


Figure 8 Variable resolution DAC with power control

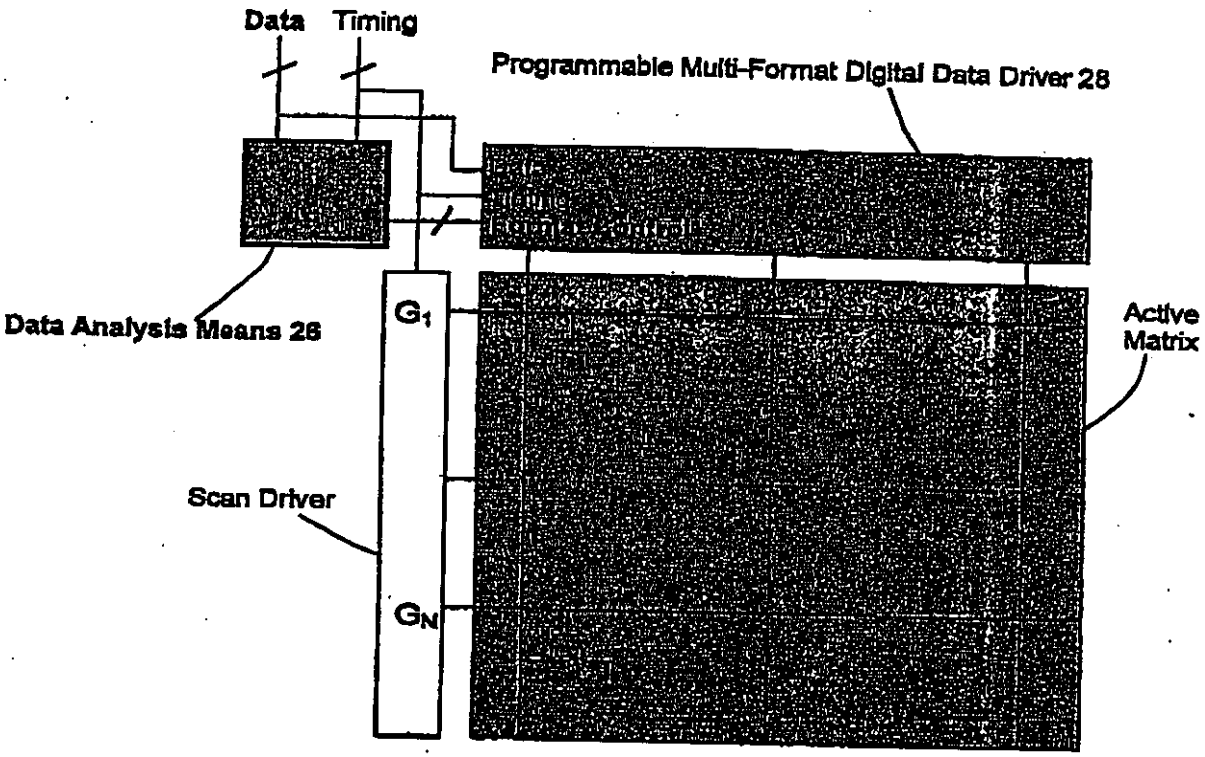


Figure 9 Basic embodiment of the invention – content driven format control

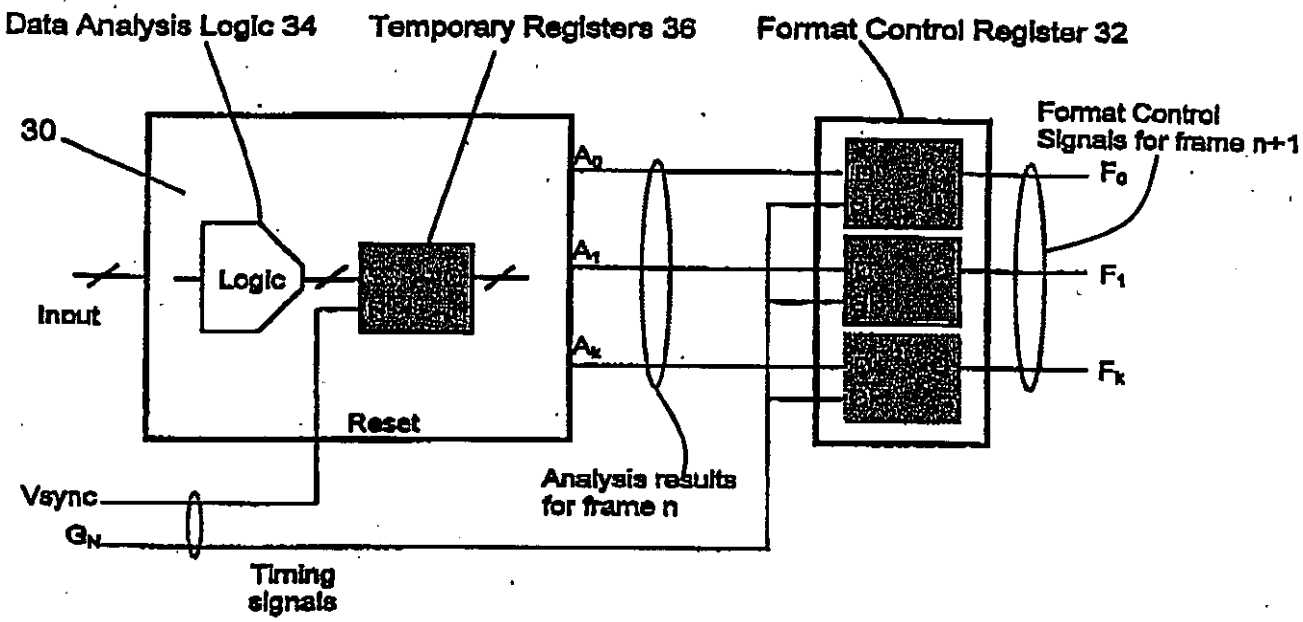


Figure 10 The functional blocks of the data analysis means

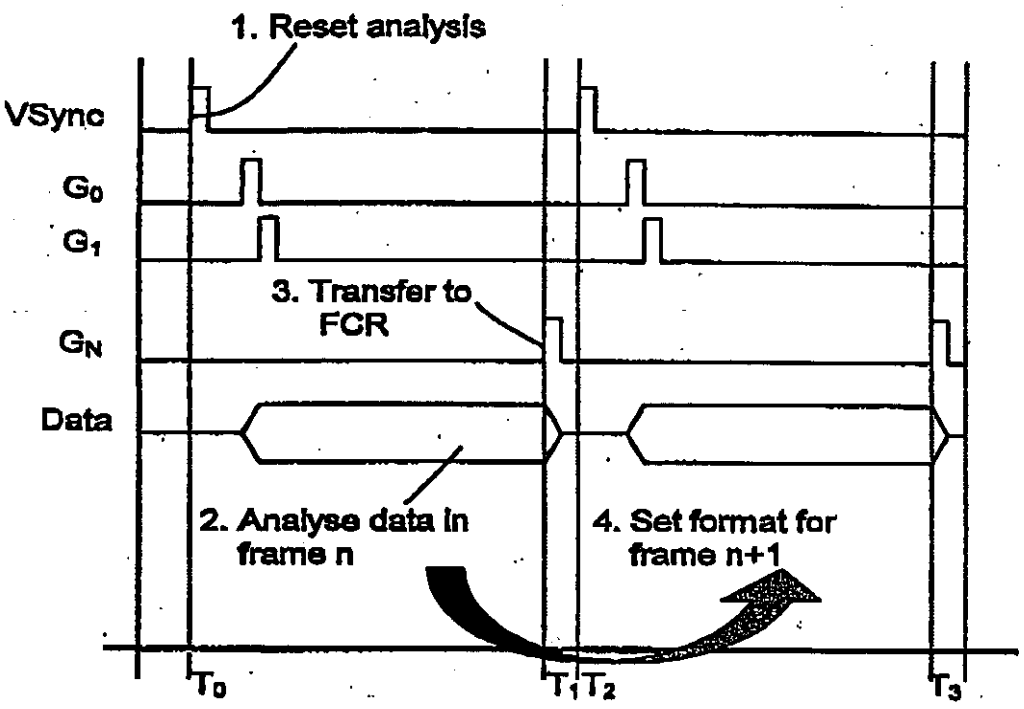


Figure 11 Generalised timing diagram for data analysis means

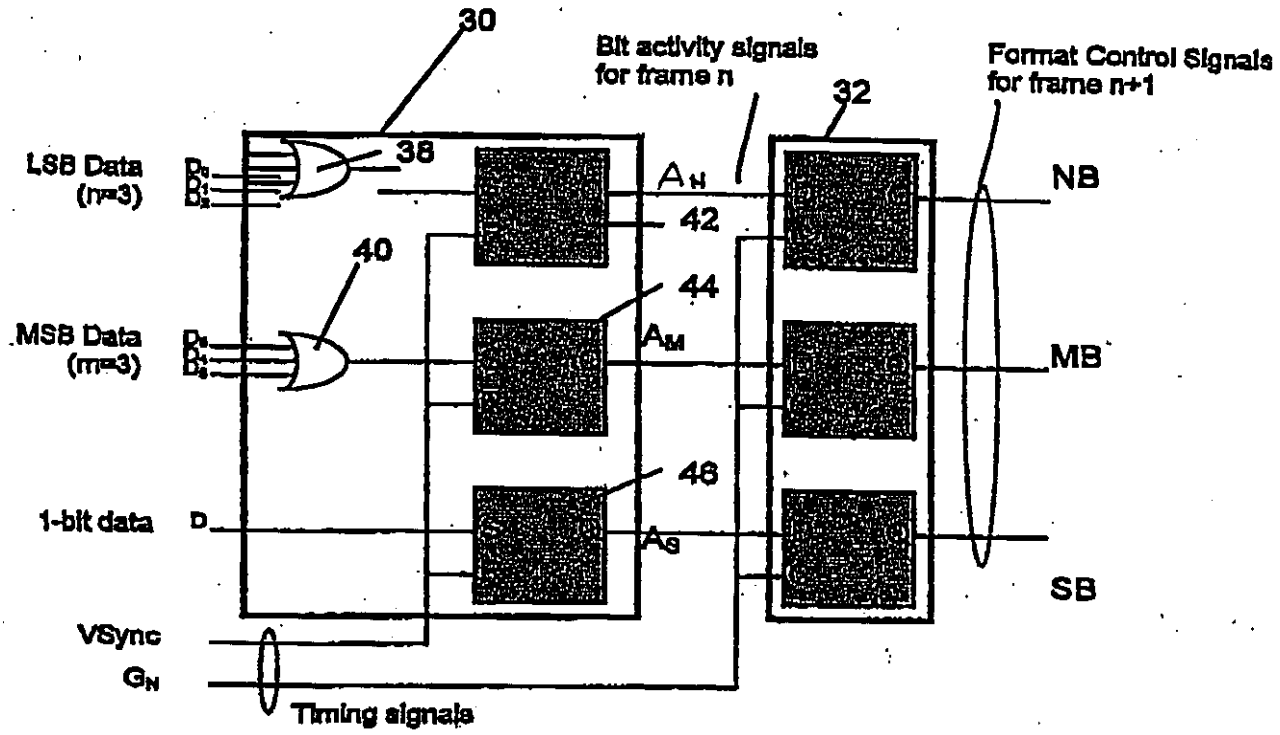


Figure 12 Embodiment of Invention – generation of bit-resolution control signals

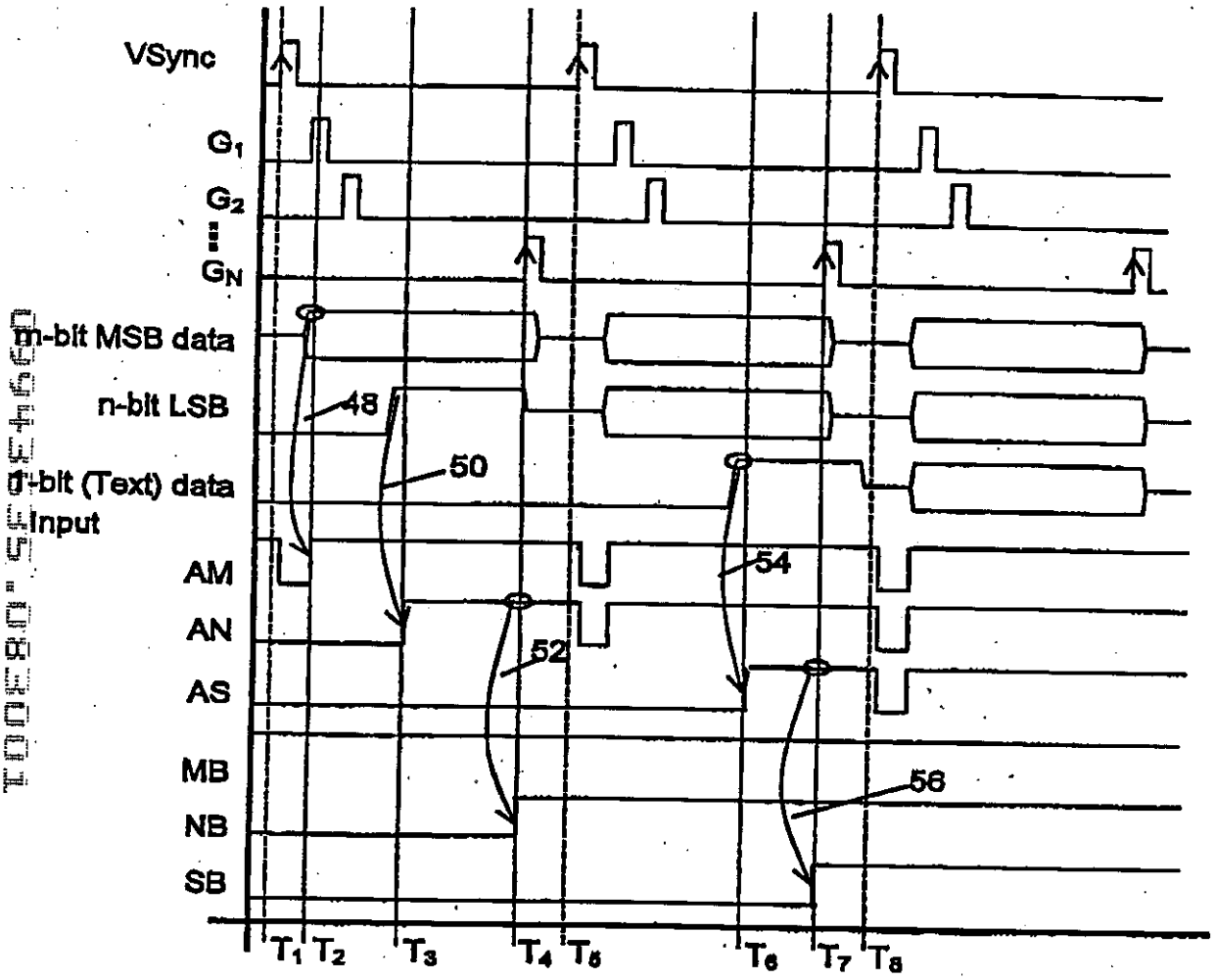


Figure 13: Timing diagram for bit-resolution embodiment

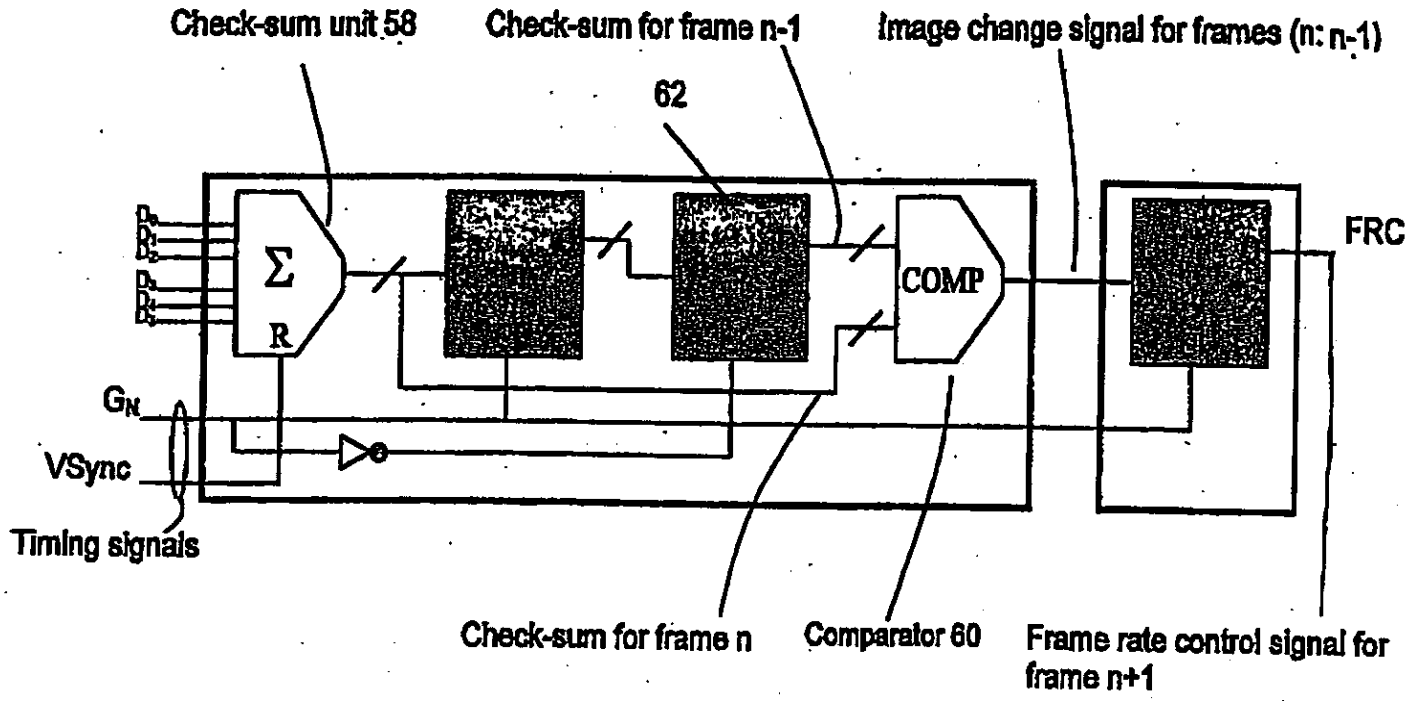


Figure 14: Embodiment of invention – analysis means for static image detection

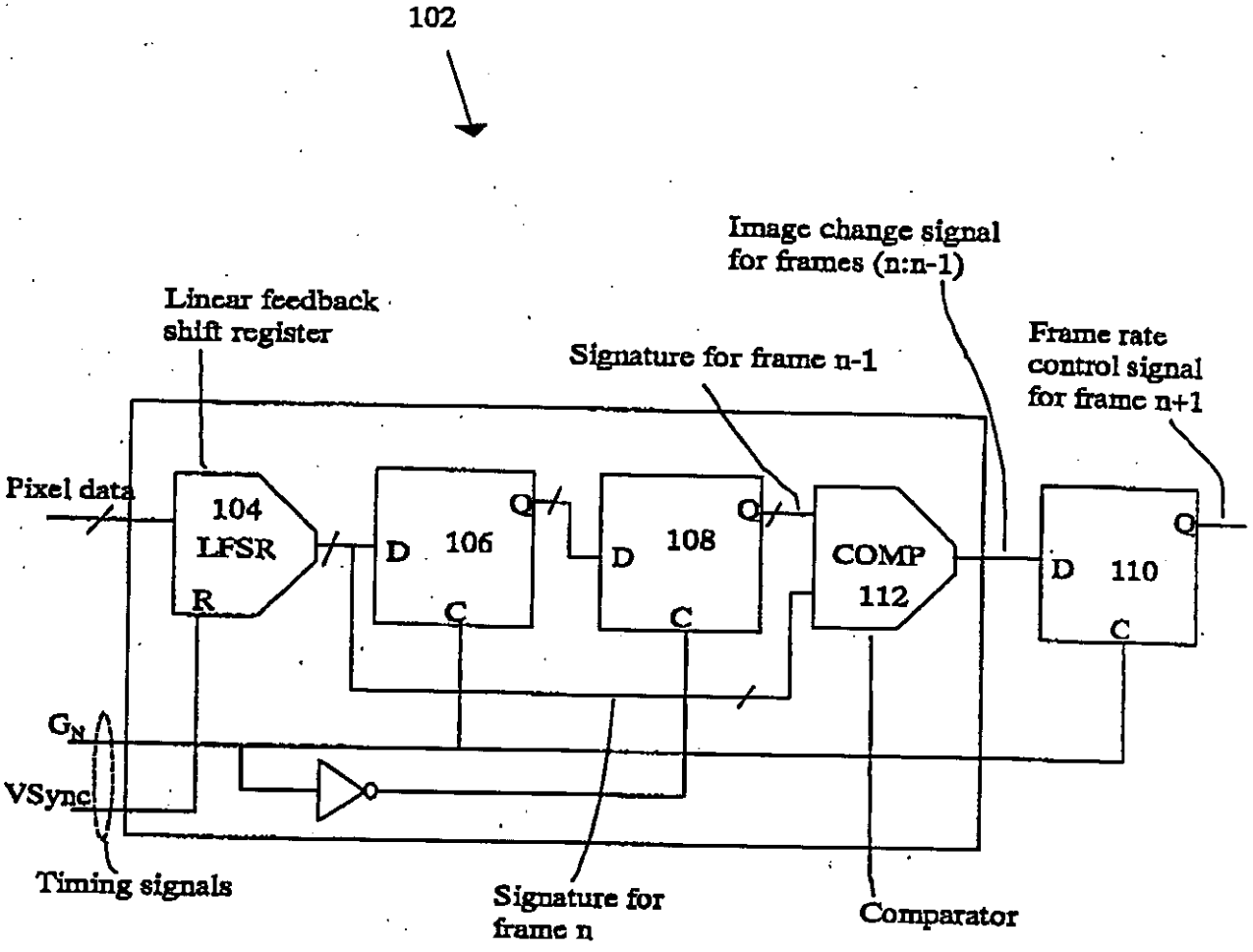
102
Image change signal for frames (n:n-1)
Linear feedback shift register
Signature for frame n-1
Frame rate control signal for frame n+1
Pixel data
104
LFSR
R
D
106
C
Q
D
108
C
Q
COMP
112
D
110
C
Q
$G_N$
VSync
Timing signals
Signature for frame n
Comparator

Figure 15

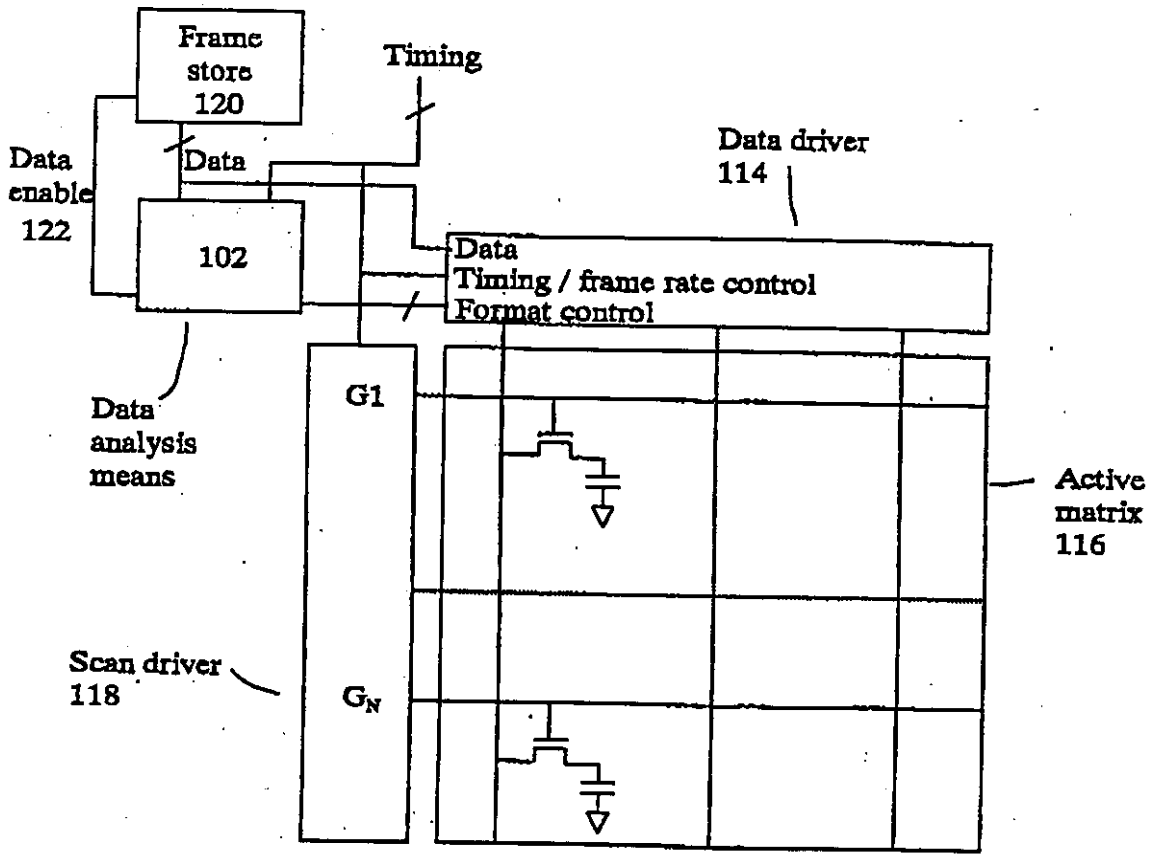


Figure 16

EP0695450

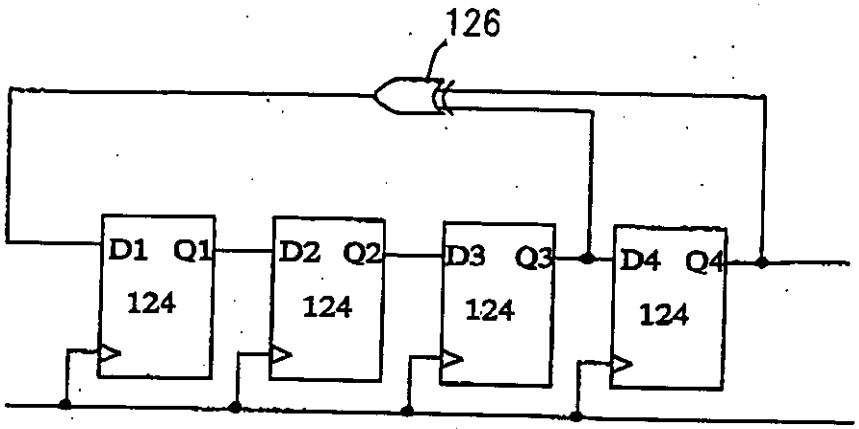


Figure 17

05454500 '09300T

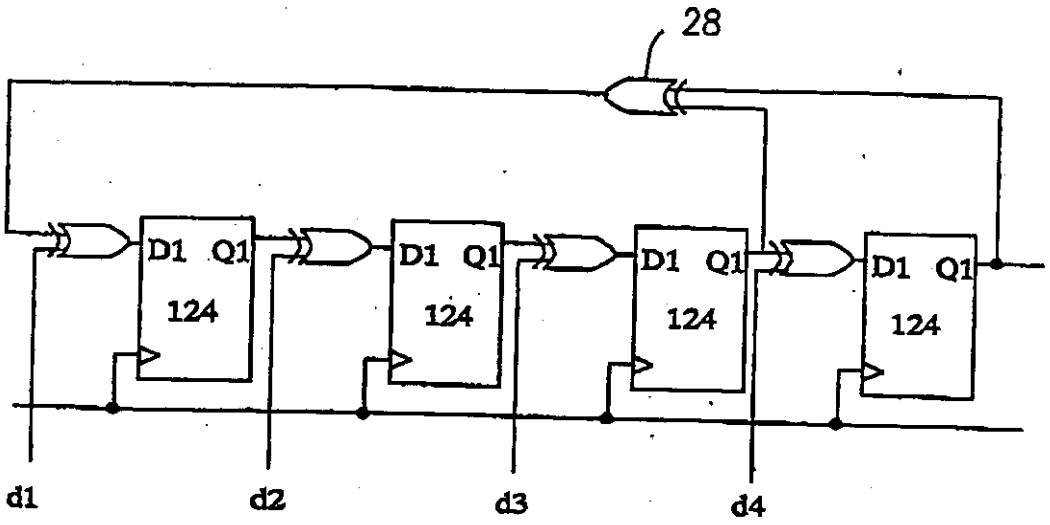


Figure 18

09543555 - 060501

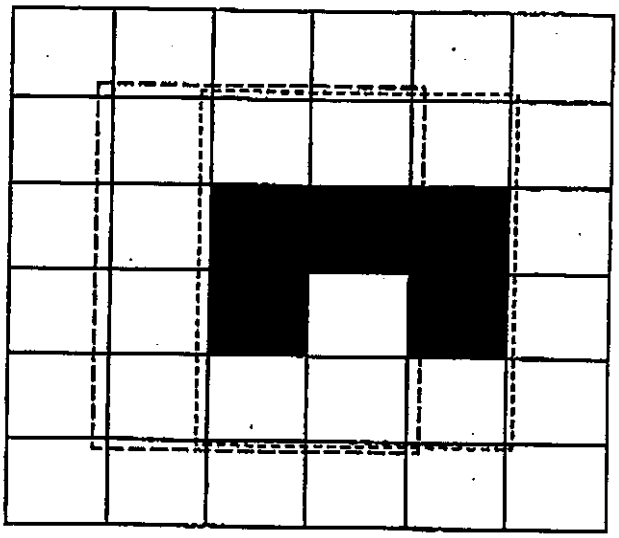

Figure 19

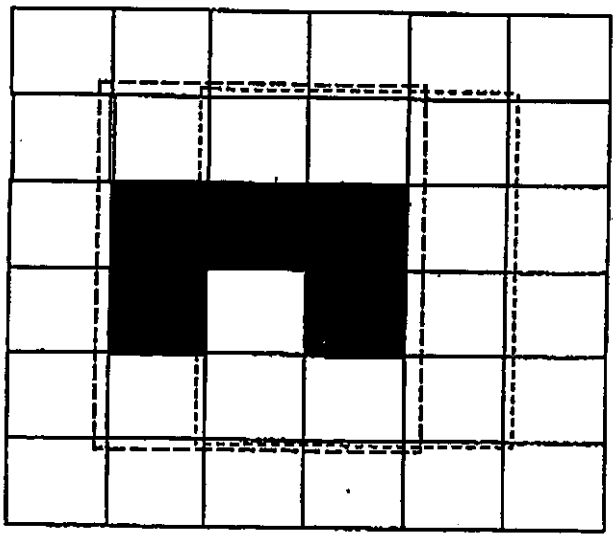

Figure 20

1000800 "05"54"650